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EXAMINER	
YUN, CARINA	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,530	KAWABATA ET AL.	
	Examiner	Art Unit	
	CARINA YUN	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendments and/or remarks filed on September 11, 2009, claims 1-25 are pending.

Response to Amendment

2. The objection to the specification has been withdrawn in light of the amendments to the specification filed on September 11, 2009. In addition, the rejection of claims 1-23, and 25 under 35 U.S.C. 101 have been withdrawn in light of the amendment to the claims filed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant cites support for amendment referring specifically to paragraph 17 of the specification. Although this section mentions latency, examiner can not see clearly how the iteration count y is determined with regards to latency time. The examiner can not find any other portion of the specification that shows support for this amendment. Examiner respectfully requests further support and explanation from applicant. Applicant is reminded of MPEP 714.02 which recites: "Applicant should also specifically point out the support for any amendments made to the disclosure. See MPEP § 2163.06." An amendment which does not comply with the

provisions of 37 CFR 1.121(b), (c), (d), and (h) may be held not fully responsive. Claims 2-23 are rejected for dependency to claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 5-6, and 23-25 are rejected under 35 U.S.C. 102(b) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Santhanam (U.S. Pat. No. 5,704,053).

Regarding claim 1, Hobbs et al. teaches a program conversion device for a processor which has an instruction set including an instruction that waits for a predetermined response from an outside source when the instruction is executed *(see Fig. 1 and also ¶ [0020] and ¶ [0021] describing the device (e.g. computer) used to perform the compilation procedures)*, comprising: a CPU (see scalar processor ¶ [0024] and Fig. 3, 200); and a compiler system including (see ¶ [0020] compiler): a loop structure transforming unit operable to perform double looping transformation so as to transform a structure of a loop *(see Fig.1 and double loop structure, see ¶ [0047])*, which is included in an input program and whose iteration count is x, into a nested structure where a loop whose iteration count is y is an inner loop and a loop whose iteration count is x/y is an outer loop *(see nested loop structure, ¶ [0047])*; and an instruction placing unit operable to convert the input program into an output program including the instruction by placing the instruction in a position outside the inner loop *(see Fig. 1; abstract and prefetch instruction outside inner loop, see ¶ [0051] and ¶ [0052])*. Hobbs does not specifically disclose wherein the iteration count y of the input program in the inner loop is determined such that processing time of the input program in the inner loop constitutes all or part of latency time of the instruction placed outside the inner loop. However, Santhanam teaches wherein the iteration count y of the input program in the inner loop is determined (see col. 8, lines 8-20 describing how the iterations are calculated) such that processing time of the input program in the inner loop constitutes all or part of latency time of the instruction placed outside the inner loop (see col. 8 lines 63 to col. 9, lines 1-7 describe how the prefetch instruction is inserted into

the loops based on the latency of loop iteration). Hence it would be obvious to combine the references of Hobbs and Santhanam in order to provide access to more accurate excepted loop interaction latency information (see col. 3, lines 47-55 of Santhanam).

Regarding claim 5, Hobbs et al. teaches the instruction is an instruction that has a possibility of causing an interlock *(see pre-fetch instruction, see ¶ [0051])*.

Regarding claim 6, Hobbs et al. that the instruction that has a possibility of causing an interlock is a prefetch instruction for prefetching data from main memory to a cache *(see 220, 230 in Fig. 3 and see ¶ [0033])*.

Regarding claim 23, Hobbs et al. teaches that the loop structure transforming unit is operable to further perform double looping transformation on an outer loop, considering an innermost loop as one block *(see ¶ [0039] describing that the loop may be transformed into separate loops with inner and outer loops, see ¶ [0047] showing example of double loop transformation)*.

Regarding claims 24 and 25, are method claims corresponding to independent claim 1, above. Therefore, these claims are rejected for the same reasons as indicated for claim 1.

8. Claims 2 and 7-14, 17-18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Santhanam (U.S. Pat. No. 5,704,053) as applied to claims 1 and 6, further in view of Nishiyama (U.S. Pat No. 6,148,439).

Regarding claim 2, Hobbs et al. teaches that the loop structure transforming unit includes: a loop detecting unit operable to detect a loop included in the input program (*i.e. identify loop in a program, see ¶ [0010]*); an iteration count detecting unit operable to detect an iteration count of the detected loop (*i.e. iteration count of j, see ¶ [0030] and ¶ [0032]*). It is noted that Hobbs

and Santhanam do not specifically disclose a response wait cycle count detecting unit operable to detect the number of response wait cycles which is the number of cycles to wait for the predetermined response when the instruction is executed; a cycles-per-sequence detecting unit operable to detect the number of cycles per sequence required for one set of iteration processing of the detected loop; a loop splitting unit operable to split off, from the detected loop, a loop whose iteration count is derived from (the number of response wait cycles/the number of cycles per sequence); and a double looping transforming unit operable to perform double looping transformation so as to build a nested structure where the loop whose iteration count is derived from (the number of response wait cycles/the number of cycles per sequence) is an inner loop and a loop whose iteration count is derived from (the iteration count of the detected loop/the iteration count of the inner loop) is an outer loop.

However, Nishiyama teaches a response wait cycle count detecting unit operable to detect the number of response wait cycles which is the number of cycles to wait for the predetermined response when the instruction is executed(*see col. 8, lines 54-59*); a cycles-per-sequence detecting unit operable to detect the number of cycles per sequence required for one set of iteration processing of the detected loop (*see col. 2, lines 44-50*); a loop splitting unit operable to split off, from the detected loop, a loop whose iteration count is derived from (the number of response wait cycles/the number of cycles per sequence) (*see col. 2, lines 50-55*); and a double looping transforming unit operable to perform double looping transformation so as to build a nested structure where the loop whose iteration count is derived from (the number of response wait cycles/the number of cycles per sequence) is an inner loop and a loop whose iteration count is derived from (the iteration count of the detected loop/the iteration count of the inner loop) is

an outer loop (*see col. 3, lines 5-24*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 7, Hobbs et al. teaches a scheduling unit operable to perform instruction scheduling (*i.e. the generator modifies the code such that the code reflects scheduling and other low-level optimization, see ¶ [0022]*). However, Hobbs and Santhanam do not specifically disclose that the loop structure transforming unit is operable to split off, from the loop whose iteration count is x, a loop whose iteration count is y and which is executed corresponding to the number of cycles required to execute the prefetch instruction, based on a result obtained by the scheduling unit, and operable to perform double looping transformation so as to build a nested structure where the loop whose iteration count is y is an inner loop and a loop whose iteration count is x/y is an outer loop.

However, Nishiyama teaches that the loop structure transforming unit is operable to split off, from the loop whose iteration count is x, a loop whose iteration count is y and which is executed corresponding to the number of cycles required to execute the prefetch instruction, based on a result obtained by the scheduling unit, and operable to perform double looping transformation so as to build a nested structure where the loop whose iteration count is y is an inner loop and a loop whose iteration count is x/y is an outer loop (*see col. 3, lines 35-45*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting

because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 8, Hobbs and Santhanam do not specifically disclose that after the instruction is executed, a plurality of cycles are required until a time comes when a predetermined resource will be referable. However, Nishiyama teaches that after the instruction is executed, a plurality of cycles are required until a time comes when a predetermined resource will be referable (*see col. 3, lines 9-18*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 9, Hobbs et al. teaches that the instruction that requires the plurality is an instruction for accessing one of main memory and a cache (*see 220 cache and 230 memory in Fig. 3 and ¶ [0024] which describes the instruction set in Fig. 3*).

Regarding claim 10, Hobbs and Santhanam do not specifically disclose that the loop structure transforming unit is operable to split off, from the loop whose iteration count is x, the loop whose iteration count is y and which is executed in accordance with an advance in a cache line size made by an address of an array referenced within the loop whose iteration count is x, and operable to perform double looping transformation so that the loop whose iteration count is y is an inner loop and the loop whose iteration count is x/y is an outer loop.

However, Nishiyama teaches that the loop structure transforming unit is operable to split off, from the loop whose iteration count is x, the loop whose iteration count is y and which is executed in accordance with an advance in a cache line size made by an address of an array

referenced within the loop whose iteration count is x, and operable to perform double looping transformation so that the loop whose iteration count is y is an inner loop and the loop whose iteration count is x/y is an outer loop (*see col. 3, lines 35-45*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 11, Hobbs and Santhanam do not specifically disclose that when a plurality of arrays are present, the loop structure transforming unit is operable to further perform, in accordance with the number of the arrays, proportional dividing transformation to proportionally divide the loop whose iteration count is y and on which the double looping transformation has been performed. However, Nishiyama teaches that when a plurality of arrays are present, the loop structure transforming unit is operable to further perform, in accordance with the number of the arrays, proportional dividing transformation to proportionally divide the loop whose iteration count is y and on which the double looping transformation has been performed (*see Fig. 15, Examiner notes a plurality of arrays are shown in the drawing, the loop is proportionally divided, see also col. 3, lines 35-45*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 12, Hobbs and Santhanam do not specifically disclose that when sizes of array elements of the plurality of arrays are different, the loop whose iteration count is y is

proportionally divided in the proportional dividing transformation in accordance with a ratio of the sizes. However, Nishiyama teaches that when sizes of array elements of the plurality of arrays are different, the loop whose iteration count is y is proportionally divided in the proportional dividing transformation in accordance with a ratio of the sizes (*see col. 3, lines 30-35*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 13, Hobbs and Santhanam do not specifically disclose that when each stride of the plurality of arrays is different, a stride referring to addresses advanced per set of the iteration processing of the loop, the loop whose iteration count is y is proportionally divided in the proportional dividing transformation in accordance with a ratio of the strides. However, Nishiyama teaches that when each stride of the plurality of arrays is different, a stride referring to addresses advanced per set of the iteration processing of the loop, the loop whose iteration count is y is proportionally divided in the proportional dividing transformation in accordance with a ratio of the strides (*see Fig. 15 and col. 3, lines 30-35; Examiner notes the arrays are different sizes, see 1501, 1502, and are proportionally divided*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 14, Hobbs and Santhanam do not specifically disclose that when an inner loop is transformed, a conditional statement is generated for each divided loop and the proportional dividing transformation is performed so that each divided loop is executed within a same inner loop. However, Nishiyama teaches that when an inner loop is transformed, a conditional statement is generated for each divided loop and the proportional dividing transformation is performed so that each divided loop is executed within a same inner loop (*see Fig. 3B, conditional IF statement*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs et al. teachings of loop optimization for better performance.

Regarding claim 17, Hobbs et al. teaches that when an execution count of a loop is non-fixed, the loop structure transforming unit is operable to judge the execution count of the loop when the loop is executed and to perform double looping transformation so as to dynamically vary an iteration count in accordance with a judgment result (*see ¶ [0052-0053]; Examiner notes the code segment shows the variable loop, the double looping transformation*).

Regarding claim 18, Hobbs et al. teaches further comprising a receiving unit operable to receive information showing that arrays are aligned to a cache line size, that the instruction placing unit is operable to place a prefetch instruction in the loop, whose iteration count is x, for prefetching data stored one cache line ahead of data to be referenced within the iteration processing of the loop that is executed x number of times (*i.e. loop optimization with prefetch, relating to size of cache memory is described. see ¶[0040] and ¶[0041]*).

Regarding claim 20, Hobbs et al. teaches that when the arrays are not aligned to the cache line size, the instruction placing unit is operable to place a prefetch instruction in the loop, whose iteration count is x, for prefetching data stored two cache lines ahead of data to be referenced within the iteration processing of the loop that is executed x number of times (*i.e. loop optimization with prefetch, relating to size of cache memory is described. see ¶[0040] and ¶[0041]*).

Regarding claim 21, Hobbs et al. teaches that when the arrays are not aligned to the cache line size, the loop structure transforming unit is operable to judge a relative position in a cache line, from which the array starts to access, and operable to perform double looping transformation in accordance with a judgment result (*see ¶ [0040]*).

Regarding claim 22, Hobbs et al. teaches further comprising a receiving unit operable to receive information that relates to a focused array (*i.e. arrays that are allocated, see ¶ [0032]*), that the loop structure transforming unit is operable to perform double looping transformation only on the focused array (*i.e. loop restructuring, see ¶ [0033]*).

9. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Santhanam (U.S. Pat. No. 5,704,053) as applied to claim 1, further in view of Ogawa et al. (U.S. Pub No. 2004/0098713 A1).

Regarding claim 3, Hobbs and Santhanam do not specifically disclose further comprising an optimization directive information receiving unit operable to receive optimization directive information which relates to optimization. However, Ogawa et al. teaches further comprising an optimization directive information receiving unit operable to receive optimization directive information which relates to optimization (*i.e. #pragma_min_iteration directive, see ¶ [0355]*).

Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include optimization directive information because Ogawa et al. teaching of optimization directive information would improve the optimization technique used for loop optimization.

Regarding claim 4, Hobbs et al. teaches the loop structure transforming unit is operable to, when an execution count of the loop is non-fixed, extract iteration processing having the minimum iteration count from the loop on the basis of the minimum iteration count and to perform double looping transformation on the extracted iteration processing of the loop (*see ¶ [0052]; Examiner notes the double loop structure is shown and minimum iteration count is 1, and loop is variable*). It is noted that Hobbs and Santhanam do not specifically disclose that the optimization directive information receiving unit is operable to receive a minimum iteration count of the loop included in the input program. However, Ogawa et al. teaches that the optimization directive information receiving unit is operable to receive a minimum iteration count of the loop included in the input program (*i.e. #pragma_min_iteration directive, see ¶ [0355]*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Santhanam to include optimization directive information because Ogawa et al. teaching of optimization directive information would improve the optimization technique used for loop optimization.

10. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Santhanam (U.S. Pat. No. 5,704,053) and Nishiyama (U.S. Pat No. 6,148,439) as applied to claim 10, and further in view of Liu et al. (U.S. Pat No. 6,070,011).

Regarding claim 15, Hobbs, Santhanam, and Nishiyama do not specifically disclose that when the loop whose iteration count is y is split off from the loop whose iteration count is x and a remainder z left over after a calculation of x/y is not zero, the loop structure transforming unit is operable to perform peeling processing and then double looping transformation on iteration processing that is to be executed z number of times. However, Liu et al. teaches that when the loop whose iteration count is y is split off from the loop whose iteration count is x and a remainder z left over after a calculation of x/y is not zero, the loop structure transforming unit is operable to perform peeling processing and then double looping transformation on iteration processing that is to be executed z number of times (*i.e. loop peeling technique used with conditional, see col. 4, lines 37-49*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hobbs, Santhanam, Nishiyama and Liu et al. because Liu et al. teaching of loop peeling would improve the loop optimization technique for better performance.

Regarding claim 16, Hobbs, Santhanam, and Nishiyama do not specifically disclose that when the remainder z is not zero, the loop structure transforming unit is operable to generate a conditional statement for judging whether a loop count of an inner loop is y or z and to perform double looping transformation. However, Liu et al. teaches that when the remainder z is not zero, the loop structure transforming unit is operable to generate a conditional statement for judging whether a loop count of an inner loop is y or z and to perform double looping transformation (*see code segment described in col. 7, lines 6-35; Examiner notes IF/ELSE conditional statement is shown, along with looping transformation*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the

teachings of Hobbs, Santhanam, Nishiyama and Liu et al. because Liu et al. teaching of loop peeling would improve the loop optimization technique for better performance.

11. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Santhanam (U.S. Pat. No. 5,704,053) and Nishiyama (U.S. Pat No. 6,148,439) as applied to claim 10, and further in view of Ogawa et al. (U.S. Pub No. 2004/0098713 A1).

Regarding claim 19, Hobbs et al. teaches the loop structure transforming unit is operable to perform the double looping transformation in accordance with the information (*see double looping transformation, ¶ [0047]*). It is noted that Hobbs, Santhanam and Nishiyama do not specifically disclose that the optimization directive information receiving unit is operable to receive information showing a relative position in a cache line, from which the array starts to access. However, Ogawa et al. teaches that the optimization directive information receiving unit is operable to receive information showing a relative position in a cache line, from which the array starts to access (*i.e. the compiler according to the present invention receives a directive on alignment for allocating array data to the memory region and performs optimization following the directive, see ¶ [0020]*). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hobbs, Santhanam, Nishiyama and Ogawa et al. because Ogawa et al. teaching of optimization directive information would improve the optimization technique used for loop optimization for better performance.

Response to Arguments

12. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARINA YUN whose telephone number is (571)270-7848. The examiner can normally be reached on Mon-Thur, 9.30am-6.30pm; alt. Fri, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SAM SOUGH can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. Y./
Examiner, Art Unit 2194

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2194
11/22/09